

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. / 10559-607001 ✓	Application No. / 10/054,179 ✓
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant William R. Wheeler et al. ✓	
		Filing Date January 17, 2002 ✓	Group Art Unit 2123 / 2825 ✓

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
[Handwritten Initials]	AA	2002/0049957	04/2002	Hosono et al.			
	AB	6,233,723	05/2001	Pribetich			
	AC	5,828,581	10/1998	Matumura			
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	AG	5,892,678	04/1999	Tokunoh et al.			
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AZ	5,506,788	04/1996	Cheng et al.				
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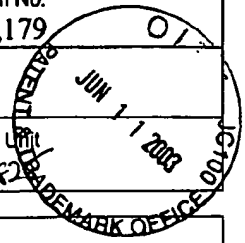
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		Filing Date January 17, 2002	Group Art Unit 242329

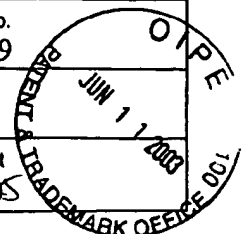


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	ADD	6,378,115	04/2002	Sakurai			
	AEE	6,272,671	08/2001	Fakhry			
	AFF	6,260,179	07/2001	Ohsawa et al.			
	AGG	6,117,183	09/2000	Teranishi et al.			
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	AOO	6,053,947	04/2000	Parson			
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	ATT	6,487,698	11/2002	Andreev et al.			
	AUU	6,311,309	10/30/2001	Southgate			
	AVV	2002/0166100	11-2002	Meding			
	AWW	US 5,629,857	05-1997	Brennan			
	AXX	2002/0046386	04-2002	Skoll et al.			
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	ABBB						

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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ACCC						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	ADDD							
	AEEE							
	AFFF							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AGGG	Foley et al., "An Object Based Graphical User Interface for Power Systems", IEEE Transactions on Power Systems, Vol. 8, No. 1, February 1993, pp. 97-104.
	AHHH	Pedram et al., "Floorplanning with Pin assignment", 1990 IEEE International Conference on Computer-Aided Design, 11 November 1990, pp. 98-101.
	AIII	Renoir, HDL Design Datasheet, Mentor Graphics, 1-8, 1999.
	AJJJ	Mentor Graphics Corporation, Renoir™ With HDL2Graphics™, pp. 1-6, 1998, Oregon.
	AKKK	Mentor Graphics Corporation, Renoir HDL Design Datasheet, pp. 1-2, 1999, Oregon.
	ALLL	Computer Design, "AFTER HARD KNOCKS, CYCLE-BASED SIMULATORS STAND THEIR GROUND". <a href="http://www.computer-design.com/Editorial/1996/10/ASIC/after.html">http://www.computer-design.com/Editorial/1996/10/ASIC/after.html</a> , accessed on August 23, 2001, pages 1-5.
	AMMM	
	ANNN	
	AOOO	

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	29 SEPTEMBER 2004
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(Revised)U.S. Department of Commerce  
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(37 CFR 1.98(b))

Applicant  
William R. Wheeler et al.Filing Date  
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	AC	4,970,664	11/1990	Kaiser, et al.			
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	AF	5,278,769	01/1994	Bair, et al.			
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	AN	5,568,397	10/1996	Yamashita, et al.			
	AO	5,598,347	01/1997	Iwasaki			
	AP	5,603,015	02/1997	Kurosawa, et al.			
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	AR	5,663,662	09/1997	Kurosawa			
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	AU	5,694,579	12/1997	Razdan, et al.			
	AV	5,706,476	01/1998	Giramma			
	AW	5,717,928	02/1998	Campmas, et al.			
	AX	5,724,250	03/1998	Kerzman, et al.			
	AY	5,757,655	05/1998	Shih, et al.			
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	AEE	5,937,190	08/1999	Gregory, et al.			
	AFF	5,974,242	10/1999	Damarla, et al.			
	AGG	6,077,304	06/2000	Kasuya			
	AHH	6,161,211	12/2000	Southgate			
	AII	6,178,541	01/2001	Joly, et al.			
	AJJ	6,208,954	03/2001	Houtchens			
	AKK	6,216,256	04/2001	Inoue, et al.			
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	AMM	6,234,658	05/2001	Houldsworth			
	ANN	6,275,973	08/2001	Wein			
	AOO	6,292,931	09/2001	Dupenloup			
	APP	6,327,693	12/2001	Cheng, et al.			
	AQQ	6,353,806	03/2002	Gehlot			
	ARR	6,353,915	03/2002	Deal, et al.			
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	ATT	6,381,563	04/2002	O'Riordan, et al.			
	AUU	6,381,565	04/2002	Nakamura			
	AVV	6,421,816	07/2002	Ishikura			
	AWW	6,438,729	08/2002	Ho			
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	AYY	6,440,780	08/2002	Kimura, et al.			
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Group Art Unit

2123

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(37 CFR 1.98(b))

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	ADDD	6,516,456	02/2003	Garnett, et al.			
	AEEE	6,519,742	02/2003	Falk			
	AFFF	6,523,156	02/2003	Cirit			
	AGGG	6,539,536	03/2003	Singh et al.			
	AHHH	6,546,528	04/2003	Sasaki, et al.			
	AIHH	6,574,787	06/2003	Anderson			
	AJJJ	6,591,407	07/2003	Kaufman, et al.			
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	ALLL	2002/0059054	05/2002	Bade, et al.			
	AMMM	2002/0112221	08/2002	Ferreri, et al.			
	ANNN	2002/0138244	09/2002	Meyer			
	AOOO	2003/0004699	01/2003	Choi, et al.			
	APPP	2003/0036871	02/2003	Fuller, et al.			
	AQQQ	2003/0177455	09/2003	Kaufman, et al.			

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Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	ARRR	0 404 482	12/1990	EPO				
	ASSS	0 433 066	06/1991	EPO				
	ATTT	0 720 233	07/1996	EPO				
	AUUU	0 901 088	03/1999	EPO				
	AVVV	1 065 611	01/2001	EPO				
	AWWW	58-060559	04/1983	Japan				
	AXXX	03-225523	10/1991	Japan				
	AYYY	07-049890	02/1995	Japan				
	AZZZ	08-314892	11/1996	Japan				

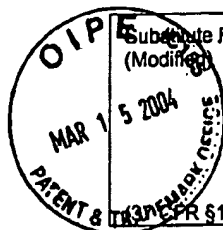
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Substitute Disclosure Form (PTO-1449)


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 Patent and Trademark Office

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(39 CFR §1.98(b))

 Applicant  
 William R. Wheeler et al.

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 January 17, 2002

Group Art Unit

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**Foreign Patent Documents or Published Foreign Patent Applications**

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AAAAA	2001-068994	03/2001	Japan				
	ABBBB	WO 98/37475	08/1998	WIPO				
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	ADDDD	WO 99/39268	08/1999	WIPO				
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	AGGGG	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
	AHHHH	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
	AIIII	Lin, et al., "A Goal Tree Based High-Level Test Planning System for DSP Real Number Models", 1998 Proceedings of International Test Conference, October 18, 1998, pp. 1000-1009.
	AJJJJ	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", <i>Electrical Design News</i> , 41(14):129-136 (1996).
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	ALLLL	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.
	AMMMM	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
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	AQQQQ	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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